REMARKS

This communication is in response to the Non-Final Office Action of December 22, 2008.

The Examiner objected to claim 25 due to informalities. Applicant has made the Examiners recommended correction.

The Examiner has rejected claims 1, 21, and 25 under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105), in view of Williams et al. (US 6,397,343), in view of Oliver et al. (US 7,243,217) and further in view of Gulick (US 6,061,802). The Examiner has rejected claims 28-30 under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105), in view of Williams et al. (US 6,397,343), in view of Oliver et al. (US 7,243,217) and further in view of Gulick (US 6,061,802), as applied to claims 1, 21 and 25 above, and further in view of Culbert et al. (US 6,820,209).

Applicant has amended the independent claims to clarify that the stalls are stalls in which one or more stages of the graphics pipeline are waiting for data inputs form upstream stages of the graphics pipeline. Applicant has also added clarifying language to clarify that the stall is in regards to the graphics pipeline. Applicant has also clarified that the performance level affects the clock rate of the graphics pipeline

The Examiner's 35 USC 103 rejection is based upon combining four references in which numerous inconsistencies and contradictions in the references are ignored. It is respectfully submitted that the Examiner is using impermissible hindsight in light of Applicant's invention and ignoring the contradictions in the references. Additionally, several of the references suffer from deficiencies such they cannot be fairly mapped to all of the elements of the amended claims. As such, it is believed that the claimed invention can not be fairly described as a combination of known elements producing a predictable results.

As one example, the Examiner is ignoring the contradictory teachings of the cited art regarding how clock speeds are controlled. Giemborek clearly teaches setting clock speeds based upon determining the amount of processing power for a display mode setting. (See, e.g., Giemborek, column 5, line 57 to column 6, line 2). Williams using the contrary technique of determining a load on a graphics subsystem. (See, e.g., Williams, Abstract).

Oliver discloses a variable speed execution pipeline in a floating point unit, not a graphics pipeline. Oliver is directed to the different problem of adjusting a clock speed according

to a level of queued opcodes – i.e., queued instructions to avoid creating "bubble instructions." (See, e.g., Oliver at Abstract and column 1, lines 61-67). However, the Examiner has overlooked that, in Oliver, the clock rate is changed for a separate execution pipeline. That is, Figure 2 of Oliver and the related text illustrates instructions (opcodes) going into circuit block 210.

Circuit block 210 has an issue block 122 and dispatch block 123 that generates control signals to execution pipe clock control block 205. However, circuit block 210 operates at a fixed clock rate, regardless of the status of the reservation stations in dispatch block 123 and the issue block 122. In particular, Oliver teaches that "[c]ircuit block 210 generally designates components of floating point unit 120 that operate at the full speed of the Input Clock Rate." (Oliver at column 4, lines 38-40). It is only the clock rate of the separate execution pipeline 124 that is varied depending on the status of opcodes in circuit block 210. That is, Oliver varies the clock rate in a different pipeline than the circuit block 210 experiencing a stall with respect to opcodes.

There is no teaching or suggestion in Oliver regarding varying the clock rate within a pipeline based upon detecting a stall within the same pipeline in regards to a stage waiting for a data input from an upstream stage. Consequently, it is respectfully submitted that it is improper to combine Oliver with the other cited art in the manner described by the Examiner. In particular, the combination would require a fundamental change in operation contrary to the principals of operation of Oliver and the other cited references.

Gulick is directed to the fundamentally different problem of synchronizing the frame rates of clocks in a plurality of data buses with respect to a master clock signal. (See, e.g., Gulick, Abstract). That is, Gulick is directed to tuning frame clocks to match a master clock. Such clock synchronization schemes are contradictory to having a variable clock rate. That is, Gulick is in a different art and directed to a fundamentally different problem than the claimed invention.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 50-1283.

Respectfully submitted,
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